ABSTRACT OF THE DISCLOSURE

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A current path pattern of semiconductor material is formed on the insulating principal surface of a substrate. A gate pattern three-dimensionally crosses the current path pattern in first and second cross areas. A channel region of the current path pattern is defined in an area superposed upon by the gate pattern. A gate insulating film is disposed between the current path pattern and gate pattern. The current path pattern has a lightly doped drain structure on both sides of the channel region in the first cross area, and is not provided with the lightly doped drain structure in regions in contact with the channel region in the second cross area. TFTs are provided having a small off-current and being not necessary for high precision position alignment during manufacture processes even if a gate length is short.